(12) UK Patent Application (19) GB (11) 2 301 202 (13) A

(43) Date of A Publication 27.11.1996

(21) Application No 9510205.9

(22) Date of Filing 19.05.1995

(51) INT CL[6]
G06F 1/32 1/04

(52) UK CL (Edition O)
G4A AFT

(56) Documents Cited
None

(58) Field of Search
UK CL (Edition N) G4A AFT
INT CL[6] G06F
Online : WPI

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(54) **Controlling processing clock signals**

(57) A data processing system is provided in which central processing unit memory and fast clock signals (mclk, fclk) to a central processing unit core (14) may be suspended to reduce power consumption. This suspension is controlled by a suspend controller (20) that responds to a write request to a predetermined address (0x0320001C) to hold asserted a bus request signal (REQ) that cooperates with a bus controller (18), and a gate disable signal (CPUSus), to block the central processing unit clock signals. The central processing unit core sees the suspend mode as a write request of an indefinite length. The suspend controller is responsive to an asynchronous input signal (FIQ, IRQ, EVENT1) to exit the suspend mode by issuing a bus acknowledge signal (ACK) and removing the block on the central processing unit clock signals. I/O can also be suspended (I/OSus), under control of a particular bit in the write request data.

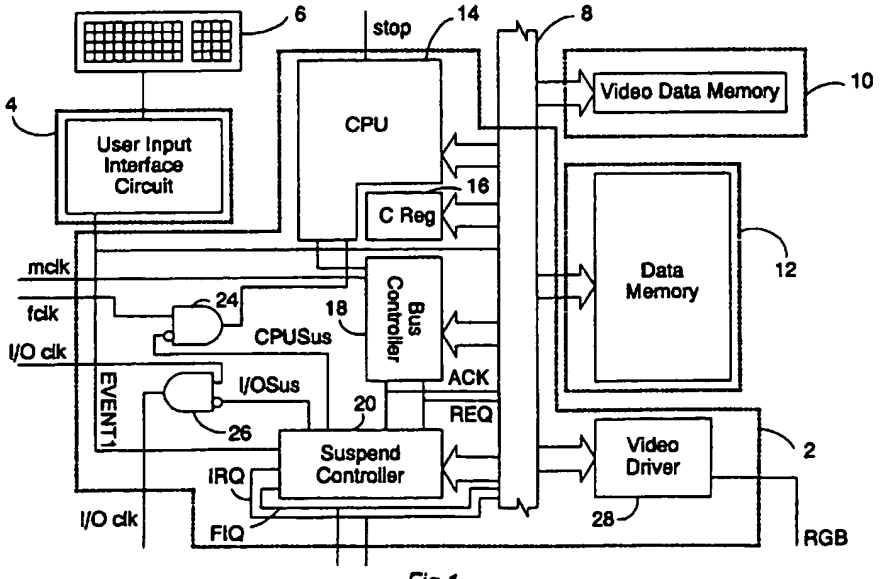

Fig.1

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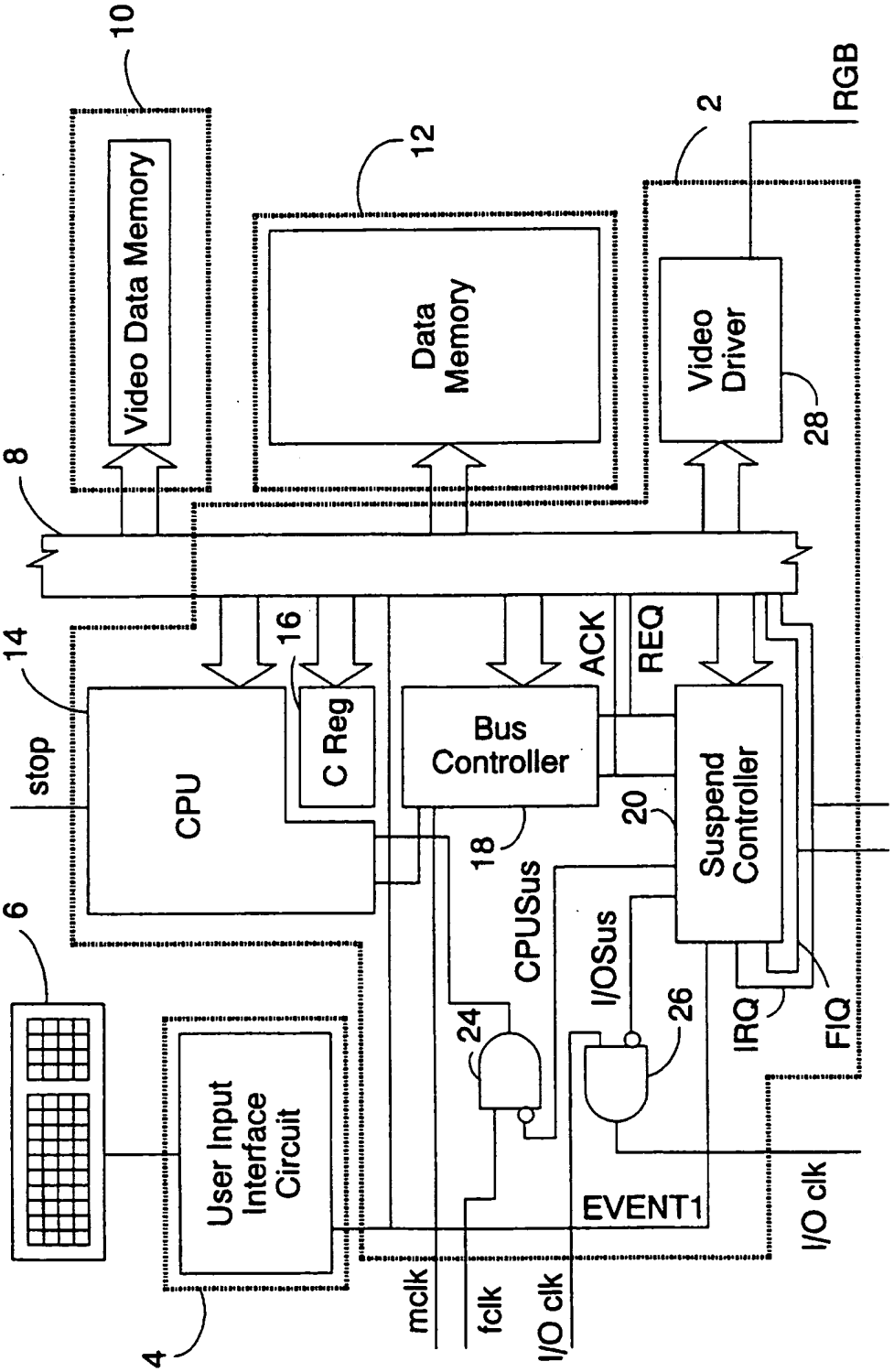

10
Video Data Memory
12
Data Memory
2
RGB
Video Driver
28
8
14
16
ACK
REQ
stop
CPU
C Reg
Bus Controller
20
Suspend Controller
18
6
CPUSus
I/OSus
24
26
IRQ
FIQ
User Input Interface Circuit
EVENT1
I/O clk
mclk
fclk
I/O clk
4

Fig. 1

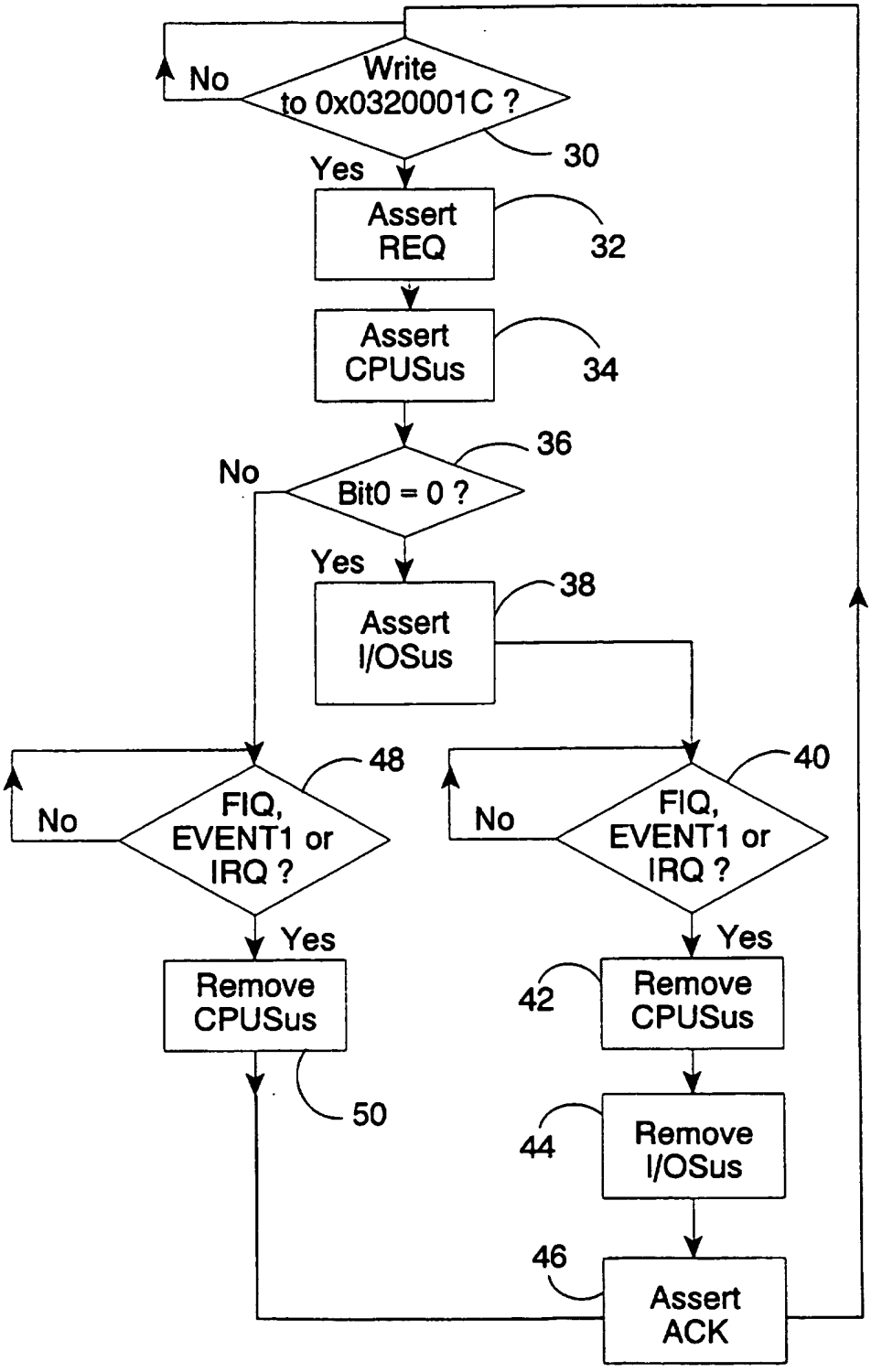

Write to 0x0320001C ?
No
Yes
30
Assert REQ
32
Assert CPUSus
34
Bit0 = 0 ?
36
No
Yes
Assert I/OSus
38
FIQ, EVENT1 or IRQ ?
48
No
Yes
Remove CPUSus
50
FIQ, EVENT1 or IRQ ?
40
No
Yes
42
Remove CPUSus
44
Remove I/OSus
46
Assert ACK

Fig.2

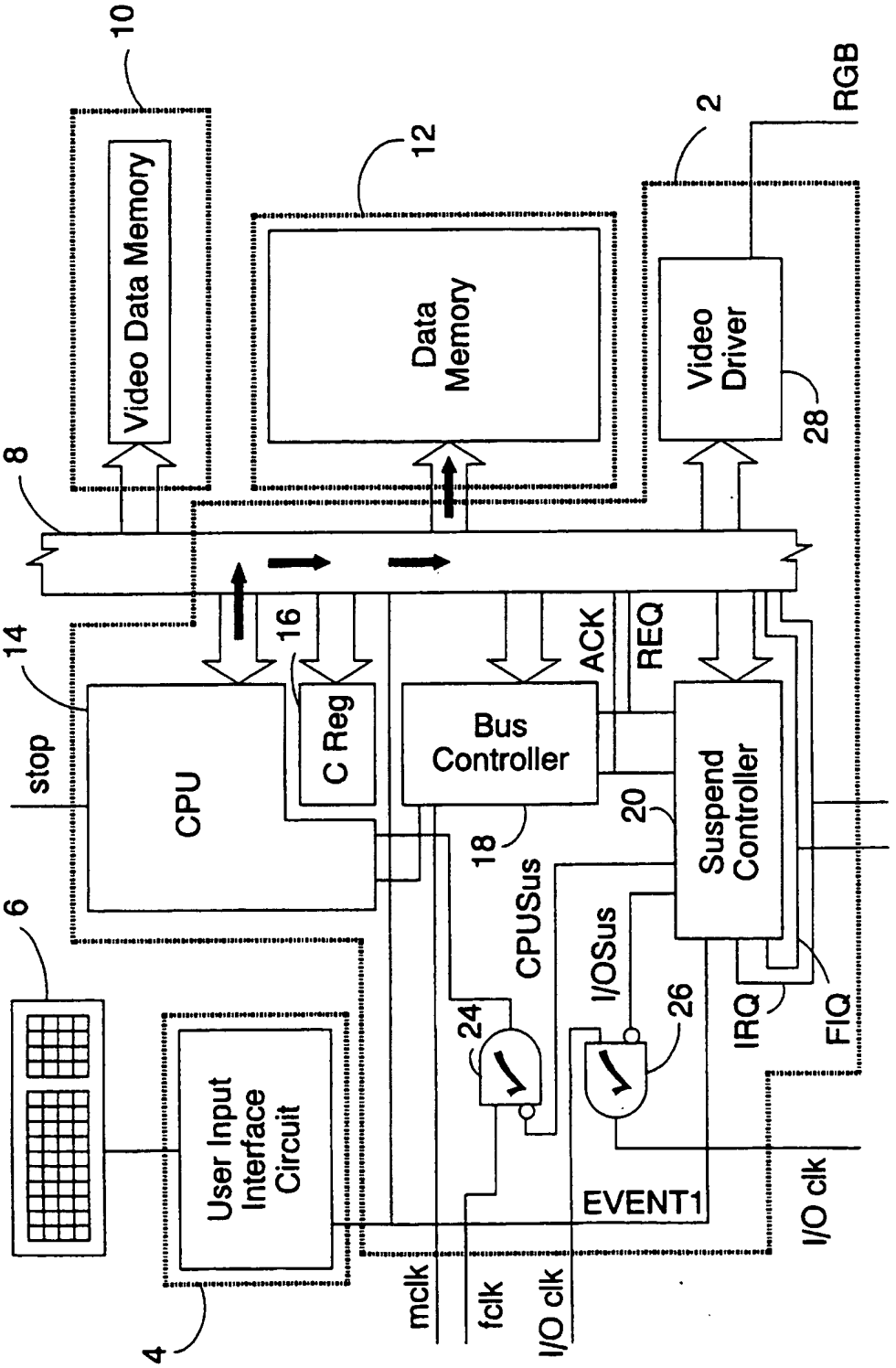
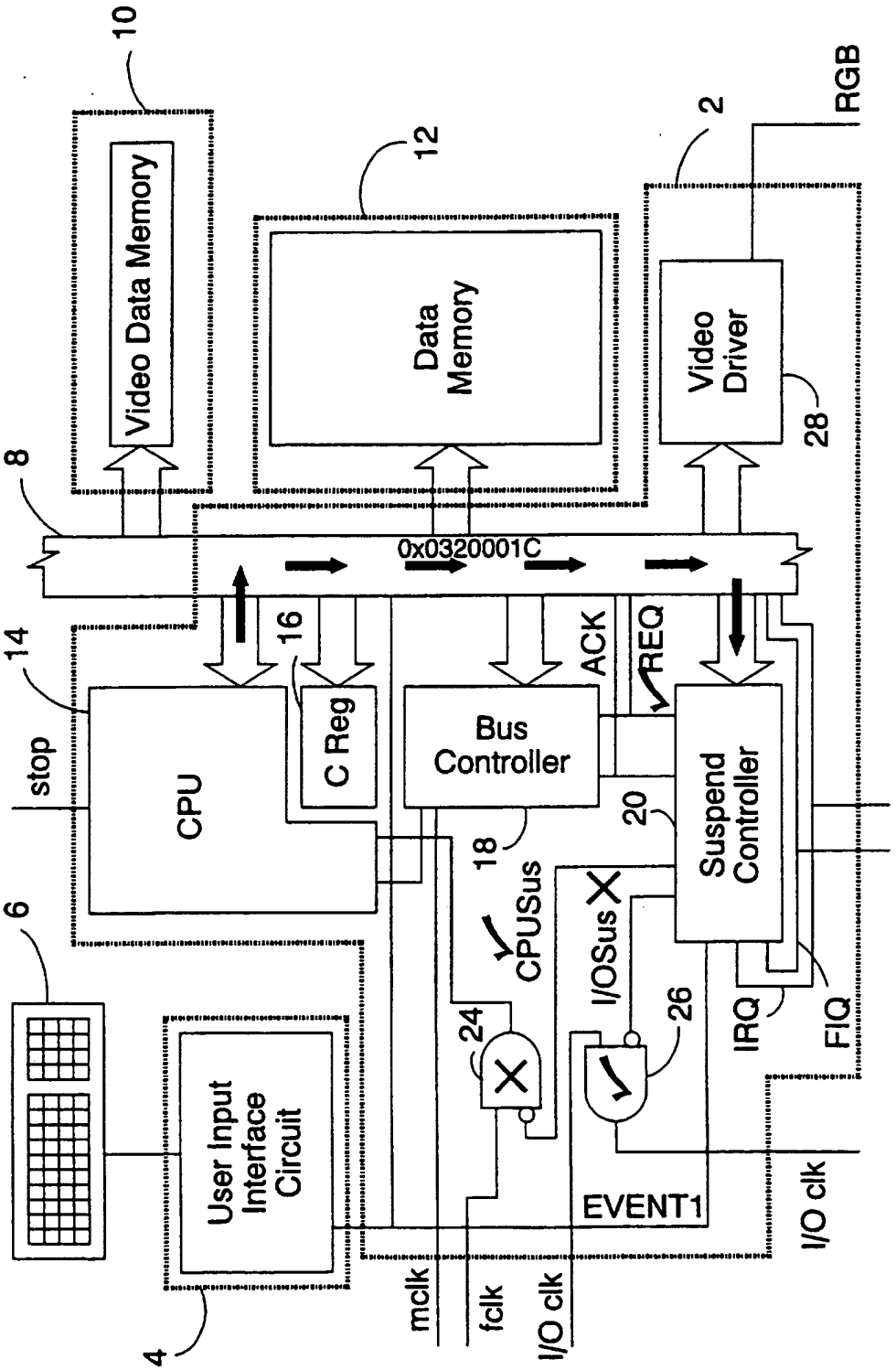

10
Video Data Memory
12
Data Memory
2
RGB
Video Driver
28
8
14
16
ACK
REQ
stop
CPU
C Reg
Bus Controller
20
Suspend Controller
18
6
CPUSus
I/OSus
24
26
IRQ
FIQ
User Input Interface Circuit
EVENT1
I/O clk
mclk
fclk
I/O clk
4

Fig.3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Video Data Memory
12
Data Memory
2
RGB
Video Driver
28
8
0x0320001C
14
16
ACK
REQ
stop
CPU
C Reg
Bus Controller
20
Suspend Controller
18
6
CPUSus
I/OSus
24
26
IRQ
FIQ
User Input Interface Circuit
EVENT1
I/O clk
mclk
fclk
I/O clk
4

Fig.4

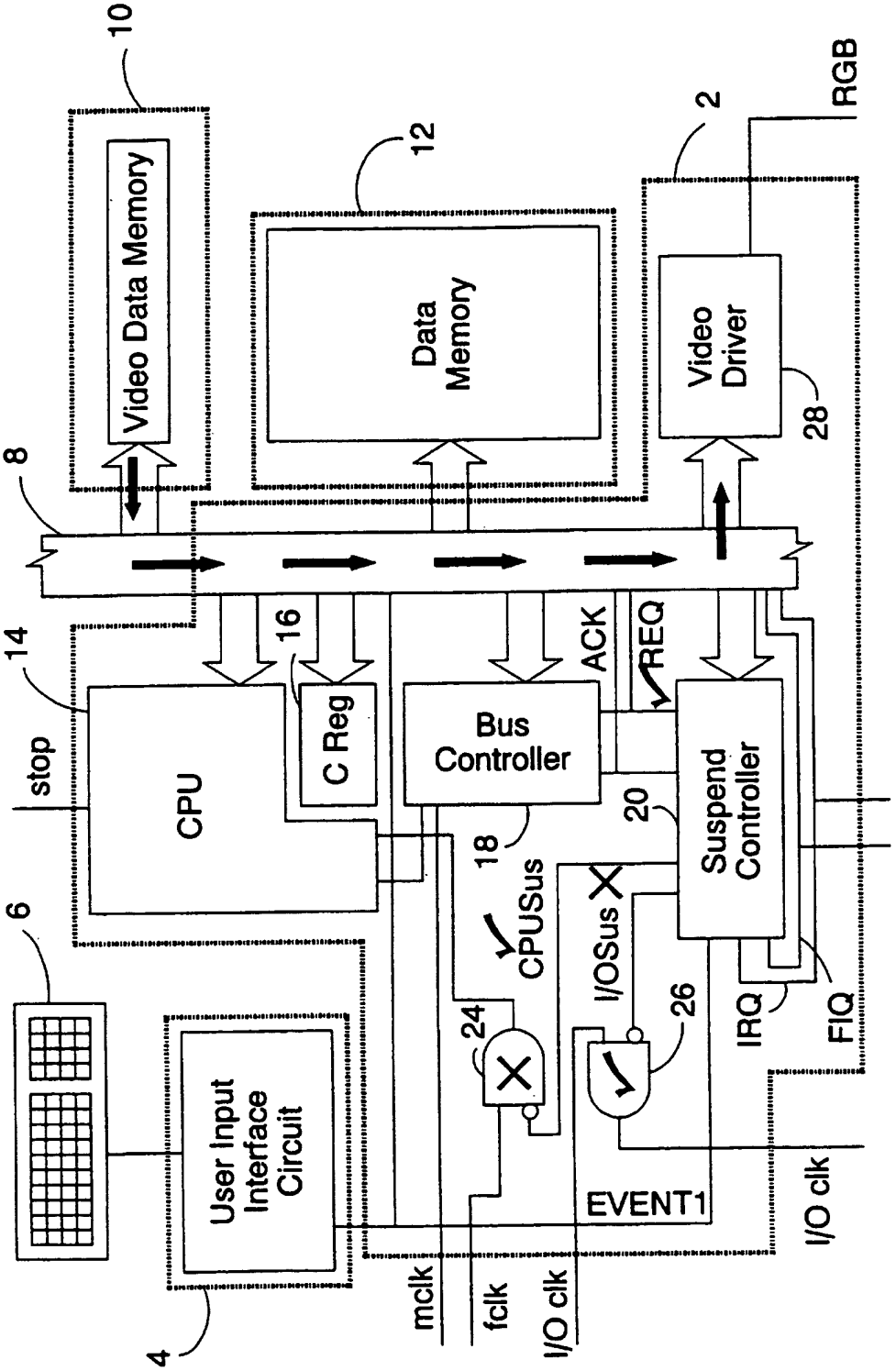
10
Video Data Memory
12
Data Memory
2
RGB
Video Driver
28
8
14
16
ACK
REQ
stop
CPU
C Reg
Bus Controller
18
20
Suspend Controller
6
CPUSus
I/OSus
24
26
IRQ
FIQ
User Input Interface Circuit
4
mclk
fclk
I/O clk
EVENT1
I/O clk

Fig.5

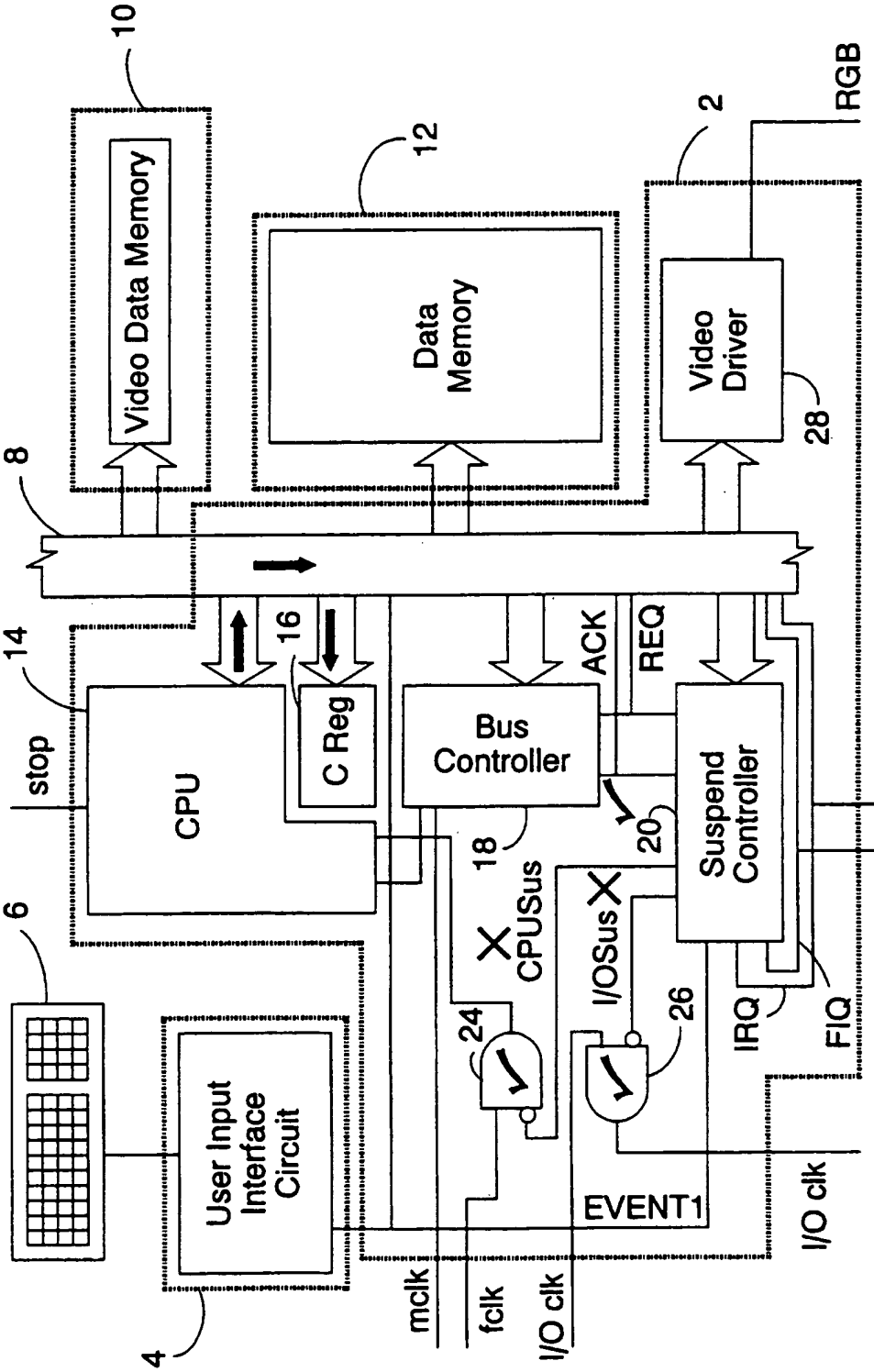
10
Video Data Memory
12
Data Memory
2
RGB
Video Driver
28
8
14
16
ACK
REQ
stop
CPU
C Reg
Bus Controller
Suspend Controller
18
20
6
CPUSus
I/OSus
24
26
IRQ
FIQ
User Input Interface Circuit
4
mclk
fclk
I/O clk
EVENT1
I/O clk

Fig.6

CONTROLLING PROCESSING CLOCK SIGNALS

This invention relates to the field of data processing systems. More particularly, this invention relates to the control of clock signals within such data processing systems.

Data processing systems include clock signals that control, regulate and drive many of the operations of the data processing apparatus. The frequency of the clock signal that is used is often a determining factor in the overall system performance since a given data processing operation may be constrained to take a fixed number of clock cycles rather than a particular time period. Accordingly, it is desirable to use as fast a clock signal as possible.

A problem with fast clock signals is that they result in an increase in power consumption. Even within the small physical size of an integrated circuit, the circuit elements and interconnecting lines have a finite capacitance resulting in a significant current flow, and consequential power consumption, as these elements and lines follow the controlling clock signal potential. This increase in power consumption within integrated circuits leads to a number of problems, e.g. potentially destructive circuit heating that requires additional heat dissipation measures to overcome.

A particular conflict between the desire for high clock speeds and other considerations arises in the field of small portable devices. With these devices available battery power is often a significant limitation and so any measures that can reduce power consumption whilst maintaining system performance are strongly advantageous.

In view of the above, specific integrated circuits have been designed for use in portable computers that allow the clock speed to be selected between a high clock speed used when significant data processing activity is required and a much lower clock speed for use when the required amount of data processing is low, e.g. the system is waiting for an input from elsewhere, such as a user input.

Whilst selectable clock speed reduces average power consumption, further reduction is advantageous.

It has been proposed in European Published Patent Application EP-A-0 562 885 to provide a system in which the clock signal supplied to a central processing unit

may be stopped in certain circumstances. In this proposed system, the central processing unit has within its instruction set a HALT instruction which acts as a busy wait state in which the clock signal is usually maintained but processing does not progress any further until an interrupt occurs.

The system proposed in EP-A-0 562 885 adds additional circuitry that detects the occurrence of such HALT commands and responds by disabling the supply of the clock signal to portions of the circuit. Thus, for those portions, the clock is stopped rather than merely slowed and an improved power consumption saving is made.

The proposed system of EP-A-0 562 885 suffers from a number of disadvantages. The system proposed in EP-A-0 562 885 assumes the existence of a HALT command within the central processing unit instruction set. Whilst the provision of such a command is not a problem when operating in a complex instruction set computing (CISC) environment, when operating in a reduced instruction set computing (RISC) environment it is disadvantageous to increase the overall size of the instruction set.

A further disadvantage of the system of EP-A-0 562 885 is that it relies upon the occurrence of interrupt signals to exit from the mode in which the clock is stopped. Interrupt signals have associated with them various interrupt handling routines and it is a disadvantageous constraint to always have to execute such an exception handling routine when restarting the clock signal. Furthermore, the need to have an interrupt to exit the clock stopped mode limits the circumstances in which the technique may be used.

Viewed from one aspect this invention provides apparatus for processing data, said apparatus comprising:

a central processing unit core driven by a central processing unit clock signal for performing data processing in response to program instructions;

an asynchronous signal input coupled to said central processing unit core for receiving asynchronous input signals;

a signal bus for transferring signals between said central processing unit core, data storage means and one or more further circuits all coupled to said signal bus;

a bus controller for controlling access to said signal bus by said central processing unit, said data storage means and said one or more further circuits and for

supplying said central processing unit clock signal to said central processing unit core;

clock suspending means responsive to a program instruction initiated write request by said central processing unit core to a predetermined address in said data storage means for issuing a request signal to said bus controller such that said bus controller suspends driving of said central processing unit core by said central processing unit clock signal whilst allowing said data storage means and said one or more further circuits to continue to communicate via said signal bus; and

clock resuming means responsive to an asynchronous input signal applied to said asynchronous signal input issuing an acknowledge signal to said bus controller such that said bus controller resumes driving of said central processing unit core by said central processing unit clock signal.

The invention overcomes the above mentioned problems by using an existing instruction within the instruction space to trigger the suspending of the central processing unit clock signal whilst allowing asynchronous input signals other than merely interrupt signals to trigger resuming of the central processing unit clock signal. Furthermore, during the suspension of the central processing unit clock signal, other circuit blocks may continue to communicate via the signal bus as appropriate.

An additional feature of the invention is that existing structure and function of the bus controller is utilised to provide operation in accordance with the invention by providing that said clock suspending means issues a write request signal to said bus controller when said central processing unit core writes to said predetermined address such that said bus controller suspends the central processing unit clock signal and thereafter waits for a write acknowledge signal before resuming the central processing unit clock signal.

In preferred embodiments of the invention said data storage means includes a video data memory and said one or more further circuits include a video driver circuit such that said video driver circuit may access and refresh said video data memory whilst driving of said central processing unit core by said central processing unit clock is suspended.

The ability for a video driver circuit to continue to be able to access the video data memory is particularly advantageous as it allows the screen display and the video data memory to be refreshed. In this way, the display can continue unaltered despite

the suspending of the central processing unit clock and a user may be unaware that the power saving feature of the invention is in operation.

As will be appreciated, the asynchronous input signals can take many different forms. However, in preferred embodiments there is provided a user input interface circuit for generating a asynchronous input signal at said asynchronous signal input in response to a user input so as to trigger resumption of driving of said central processing unit core by said central processing unit clock signal.

It is often the case that the central processing unit core will have little data processing to perform whilst it is waiting for the next user input. Accordingly, the suspending of the central processing unit clock whilst awaiting for the next user input signal is strongly advantageous.

In preferred embodiments of the invention said user input interface circuit comprises a keyboard interface circuit and wherein said central processing unit core and said bus controller together act to suspend said central processing unit clock whilst waiting for a keyboard input signal to said keyboard interface circuit.

The power savings available from the invention and the manner in which the suspend mode may be entered and exited make it possible to suspend the central processing unit core between individual key strokes as a power saving measure.

Whilst suspending the clock signal to the central processing unit core saves a considerable amount of power, still further power can be saved in preferred embodiments in which said clock suspending means suspends a further circuit clock signal driving one or more of said further circuits when suspending said central processing unit clock signal and said clock resuming means resumes said further circuit clock signal when resuming said central processing unit clock signal.

In contrast to the previously proposed system discussed above, preferred embodiments of the invention allow an additional degree of sophistication in the control of the clock signals by providing that said clock suspending means selectively suspends said further circuit clock signal in dependence upon a data value written to said predetermined address.

Whilst the invention may be used in systems having only one type of asynchronous input signal, it is preferable that the system includes a plurality of asynchronous input signals that may serve to resume the central processing unit clock

signal.

When the central processing unit clock signal is suspended, e.g. whilst expecting a user input, it is important that the system should still be responsive to interrupts. Accordingly, preferred embodiments of the invention further comprise one or more interrupt signal inputs coupled to said central processing unit core for receiving interrupt signals, said clock resuming means being responsive to received interrupt signals to resume said central processing unit clock signal and said central processing unit core being responsive to received interrupt signals to initiate an interrupt handling routine.

Whilst certain of the circuit elements of the invention could be fabricated separately, it is preferable that said central processing unit core, said bus controller, said clock suspending means and said clock resuming means are formed as a central processing unit integrated circuit.

It will be appreciated that data storage means (e.g. any devices corresponding to a portion of the address space) may take many different forms, e.g. a DRAM, a SRAM, a VRAM, ..., but by virtue of the particular special properties associated with the predetermined address within the data storage means it is preferable that said data storage means includes a data register, said predetermined address corresponding to said data register.

Whilst the data storage means can be considered as the full memory address space of the system, it will be appreciated that this is usually sub-divided. In preferred embodiments of the invention said data storage means includes a random access memory, said random access memory being formed as a random access memory integrated circuit coupled to said central processing unit core, said bus controller, said clock suspending means and said clock resuming means.

As previously mentioned, the ability to control which of the various clock signals within the system are suspended in dependence upon the data value written to the predetermined address is advantageous, this is particularly so when said further circuit clock signal is an input/output device clock signal that is supplied at an external pin of said central processing unit integrated circuit.

An input/output device clock signal that is driven off-chip can consume a particularly large amount of power due to the relatively high capacitance of such off-

chip lines.

If still further power saving is desired, then preferred embodiments may provide this when said central processing unit core is responsive to predetermined program instructions to assert a stop signal that stops clock signal generation such that no communication may take place via said signal bus.

Such a stop mode is more drastic than the suspend mode previously discussed and will generally produce a noticeable effect to the user, e.g. a lack of screen refresh or a longer time to recover the system back to the fully operational state.

Such an approach makes modification of an existing design possible rather than having to re-engineer the system more comprehensively.

Whilst the clock suspending means and the clock resuming means may be separately embodied, in preferred embodiments these two entities are provided as a suspend controller circuit block.

Viewed from another aspect the invention provides a method of processing data, said method comprising the steps of:

driving a central processing unit core by a central processing unit clock signal for performing data processing in response to program instructions;

receiving asynchronous input signals at an asynchronous signal input coupled to said central processing unit core;

transferring signals via a signal bus between said central processing unit core, a data memory and one or more further circuits all coupled to said signal bus; and

controlling with a bus controller access to said signal bus by said central processing unit, said data memory and said one or more further circuits;

supplying said central processing unit clock signal from said bus controller to said central processing unit core;

responding to a program instruction initiated write request by said central processing unit core to a predetermined address in said data storage means by issuing a request to said bus controller such that said bus controller suspends driving of said central processing unit core by said central processing unit clock signal whilst allowing said data storage means and said one or more further circuits to continue to communicate via said signal bus; and

responding to an asynchronous input signal applied to said asynchronous signal

input by issuing an acknowledge signal to said bus controller such that said bus controller resumes driving of said central processing unit core by said central processing unit clock signal.

An embodiment of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 illustrates a data processing system in which the central processing unit clock may be suspended;

Figure 2 is a flow diagram illustrating the functional flow of suspending and resuming the central processing unit clock of Figure 1; and

Figures 3 to 6 illustrate various modes of operation of the system of Figure 1.

Figure 1 illustrates a central processing unit integrated circuit 2 connected via a user input interface circuit 4 to a keyboard 6 and via a signal bus 8 to a video data memory 10 and a random access memory 12. The central processing unit integrated circuit 2 receives inputs that include a memory clock signal mclk, a fast clock signal fclk and an input/output clock signal I/O clk. The signal bus 8 extends outside of the central processing unit integrated circuit 2 such that the video data memory 10 and random access memory 12 may communicate address and data words with the rest of the system. A fast interrupt signal FIQ and a slow interrupt signal IRQ are also input to the central processing unit integrated circuit 2 along with a first asynchronous event signal EVENT1 from the user input interface circuit 4. The I/O clk signal is driven out from the central processing unit integrated circuit 2 and serves to supply additional I/O circuits, such as hard disc controllers and the like. A stop signal is input that serves to freeze the central processing unit integrated circuit 2 completely.

Within the central processing unit integrated circuit 2 there is a central processing unit core 14 that contains the main processing circuit elements, such as the instruction pipeline, instruction decoder and processing logic. The central processing unit core 14 is coupled to the signal bus 8. A control register bank 16 containing the control registers and status flags for the integrated circuit 2 communicates with the central processing unit core 14 via the signal bus 8. A bus controller 18 is coupled to the signal bus 8 to provide co-ordination and arbitration between bus communication operations using bus request REQ and bus acknowledge ACK signals. A suspend controller 20 is coupled to the signal bus 8 and additionally receives the

interrupt signals FIQ and IRQ and the asynchronous event signal EVENT1. The suspend controller 20 serves to generate pseudo bus request REQ and bus acknowledge ACK signals as well as a CPUSus signal and a I/OSus signal. AND gates 24 and 26 with one inverted input receive the fast clock signal fclk and input/output signal I/O clk as well as the CPUSus and I/OSus signals.

A video driver circuit 28 within the central processing unit integrated circuit 2 serves to generate an RGB signal in response to display data received from the video data memory 10 via the signal bus 8.

Figure 2 illustrates the operation of the suspend controller 20 of Figure 1. At step 30, the suspend controller 20 monitors the signal bus 8 to detect a write request to address 0x0320001C (0x indicates that the following number is hexidecimal). The address 0x0320001C is within the address space normally reserved for control registers, although a physical register need not necessarily be provided.

When such a write request is detected at step 30, steps 32 and 34 serve to hold asserted the (pseudo) bus request signal REQ and the CPUSus signal. The CPUSus signal acts on the AND gate 24 to block the supply of the fast clock signal fclk to the central processing unit core 14 whilst the bus request signal REQ causes the bus controller 18 to block the memory clock signal mclk. Accordingly, the assertion of the bus request signal REQ and the stopping of the central processing unit clock to the central processing unit core 14 has the result that the central processing unit 14 maintains a fixed state, so saving a significant amount of power, and the bus controller 18 sees what appears to be a long bus request signal REQ.

At step 36, the suspend controller 20 determines the value of the least significant bit Bit0 of the data value being written to address 0x0320001C. If this bit is a "0" then this indicates that the input/output clock signal I/O clk should also be suspended (otherwise this signal is not suspended). If Bit0 = 0, then the I/OSus signal is asserted at step 38. The I/OSus signal acts with the AND gate 26 to block the supply of the I/O clk signal.

At step 40, the suspend controller 20 monitors for an asynchronous input signal that may be a fast interrupt FIQ, a slow interrupt IRQ or an asynchronous event signal EVENT1. When such a signal occurs, steps 42 and 44 remove the blocking of the central processing unit clock signals and the I/O clock signal by the AND gates 24

and 26.

Step 46 serves to assert the bus acknowledged signal ACK that causes the bus controller 18 to unblock the memory clock signal mclk.

If at step 36 the determination was Bit0 = 1, then step 48 monitors for the occurrence of an asynchronous input signal and step 50 serves to remove the CPUSus signal before passing control to step 46.

Figure 3 illustrates the operation of the system of Figure 1 in one of its normal modes. In this mode, both the memory clock signal mclk and the fast clock signal fclk are enabled to the central processing unit core 14. The central processing unit core 14 makes a selection between these two clock signals as to which one to internally utilise depending upon the nature of the operation being performed by the central processing unit core at that point in time. The I/O clk signal is also enabled. A write request from the central processing unit core 14 to the random access memory 12 is passed by the signal bus 8 that carries both the address word and the data words. At the start of this bus communication operation, a bus request signal REQ is issued by a memory controller (not shown) to the bus controller 18 that then allocates the signal bus to that bus communication operation until it is completed, at which time a bus acknowledge signal ACK is issued to release the signal bus 8 for use by other circuit elements.

Figure 4 illustrates entry of the suspend mode. The central processing unit core 14 issues a write request to address 0x0320001C. The suspend controller 20 recognises this write request and asserts and holds the (pseudo) bus request signal REQ supplied to the bus controller 18. The suspend controller also asserts the CPUSus signal that blocks the supply of the fast clock signal fclk to the central processing unit core 14. In this case, the value of the word being written by the central processing unit core 14 has as its least significant bit (Bit0) a "1" and accordingly, the I/O clk signal is not suspended.

Figure 5 illustrates the manner in which the clock signal to the central processing unit core 14 may be blocked, so saving power, whilst allowing other circuit elements, such as the video driver circuit 10 and the video data memory 28 to continue to communicate via the signal bus. Such communication allows the video data memory 10 to supply the video data memory 28 and so provide a continuous

display output to the user.

Figure 6 illustrates the exiting of the suspend mode. A keystroke at the keyboard 6 is detected by the user input interface circuit 4 which then issues an asynchronous event signal EVENT1 that is supplied to the suspend controller 20. The suspend controller 20 reacts by removing the bus request signal REQ and the CPUSus signal and then asserting the (pseudo) bus acknowledge signal ACK. The action of removing the CPUSus signal allows the fast clock signal fclk to again be supplied to the central processing unit core 14. The bus acknowledge signal ACK also unblocks the memory clock signal mclk by the bus controller. The central processing unit core 14 sees the suspend mode as a single write operation of an indefinite length. Having exited the suspend mode, the central processing unit core 14 is again supplied with a clock signal and can recommence operation, such as communicating via the signal bus 8 with the control registers 16 to perform data processing.

CLAIMS

1. Apparatus for processing data, said apparatus comprising:

a central processing unit core driven by a central processing unit clock signal for performing data processing in response to program instructions;

an asynchronous signal input coupled to said central processing unit core for receiving asynchronous input signals;

a signal bus for transferring signals between said central processing unit core, data storage means and one or more further circuits all coupled to said signal bus;

a bus controller for controlling access to said signal bus by said central processing unit, said data storage means and said one or more further circuits and for supplying said central processing unit clock signal to said central processing unit core;

clock suspending means responsive to a program instruction initiated write request by said central processing unit core to a predetermined address in said data storage means for issuing a request signal to said bus controller such that said bus controller suspends driving of said central processing unit core by said central processing unit clock signal whilst allowing said data storage means and said one or more further circuits to continue to communicate via said signal bus; and

clock resuming means responsive to an asynchronous input signal applied to said asynchronous signal input issuing an acknowledge signal to said bus controller such that said bus controller resumes driving of said central processing unit core by said central processing unit clock signal.

2. Apparatus as claimed in claim 1, wherein said data storage means includes a video data memory and said one or more further circuits include a video driver circuit such that said video driver circuit may access and refresh said video data memory whilst driving of said central processing unit core by said central processing unit clock is suspended.

3. Apparatus as claimed in any one of claims 1 and 2, comprising a user input interface circuit for generating an asynchronous input signal at said asynchronous signal input in response to a user input so as to trigger resumption of driving of said

central processing unit core by said central processing unit clock signal.

4. Apparatus as claimed in claim 3, wherein said user input interface circuit comprises a keyboard interface circuit and wherein said central processing unit core and said bus controller together act to suspend said central processing unit clock whilst waiting for a keyboard input signal to said keyboard interface circuit.

5. Apparatus as claimed in any one of the preceding claims, wherein said clock suspending means suspends a further circuit clock signal driving one or more of said further circuits when suspending said central processing unit clock signal and said clock resuming means resumes said further circuit clock signal when resuming said central processing unit clock signal.

6. Apparatus as claimed in claim 5, wherein said clock suspending means selectively suspends said further circuit clock signal in dependence upon a data value written to said predetermined address.

7. Apparatus as claimed in any one of the preceding claims, comprising a plurality of asynchronous signal inputs for receiving a plurality of asynchronous input signals that may serve to resume said central processing unit clock signal.

8. Apparatus as claimed in any one of the preceding claims, further comprising one or more interrupt signal inputs coupled to said central processing unit core for receiving interrupt signals, said clock resuming means being responsive to received interrupt signals to resume said central processing unit clock signal and said central processing unit core being responsive to received interrupt signals to initiate an interrupt handling routine.

9. Apparatus as claimed in any one of the preceding claims, wherein said central processing unit core, said bus controller, said clock suspending means and said clock resuming means are formed as a central processing unit integrated circuit.

10. Apparatus as claimed in any one of the preceding claims, wherein said data storage means includes a data register, said predetermined address corresponding to said data register.

11. Apparatus as claimed in claim 9 and 10, wherein said data storage means includes a random access memory, said random access memory being formed as a random access memory integrated circuit coupled to said central processing unit core, said bus controller, said clock suspending means and said clock resuming means.

11. Apparatus as claimed in claims 6 and 9, wherein said further circuit clock signal is an input/output device clock signal that is supplied at an external pin of said central processing unit integrated circuit.

12. Apparatus as claimed in any one of the preceding claims, wherein said central processing unit core is responsive to predetermined program instructions to assert a stop signal that stops clock signal generation such that no communication may take place via said signal bus.

13. Apparatus as claimed in any one of the preceding claims, wherein said clock suspending means and said clock resuming means comprises a suspend controller circuit block.

14. A method of processing data , said method comprising the steps of:

driving a central processing unit core by a central processing unit clock signal for performing data processing in response to program instructions;

receiving asynchronous input signals at an asynchronous signal input coupled to said central processing unit core;

transferring signals via a signal bus between said central processing unit core, a data memory and one or more further circuits all coupled to said signal bus; and

controlling with a bus controller access to said signal bus by said central processing unit, said data memory and said one or more further circuits;

supplying said central processing unit clock signal from said bus controller to

said central processing unit core;

responding to a program instruction initiated write request by said central processing unit core to a predetermined address in said data storage means by issuing a request to said bus controller such that said bus controller suspends driving of said central processing unit core by said central processing unit clock signal whilst allowing said data storage means and said one or more further circuits to continue to communicate via said signal bus; and

responding to an asynchronous input signal applied to said asynchronous signal input by issuing an acknowledge signal to said bus controller such that said bus controller resumes driving of said central processing unit core by said central processing unit clock signal.

15. Apparatus for processing data substantially as hereinbefore described with reference to the accompanying drawings.

16. A method of processing data substantially as hereinbefore described with reference to the accompanying drawings.

Patents Act 1977 Examiner's report to the Comptroller under Section 17 (The Search report) 15	Application number GB 9510205.9
Relevant Technical Fields (i) UK Cl (Ed.N) G4A (AFT) (ii) Int Cl (Ed.6) G06F	Search Examiner M J DAVIS Date of completion of Search 19 JULY 1995
Databases (see below) (i) UK Patent Office collections of GB, EP, WO and US patent specifications. (ii) ONLINE: WPI	Documents considered relevant following a search in respect of Claims :- 1-16

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A:	Document indicating technological background and/or state of the art.	**&:**	Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages	Relevant to claim(s)
	NONE	

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